

## **AMENDMENTS TO THE CLAIMS**

The following listing of claims will replace all prior versions and listings of claims in the application.

### **LISTING OF CLAIMS**

1. (Currently Amended) A semiconductor substrate comprising:  
an SOI structure including a single-crystal silicon layer for forming a device formed on an insulating layer;  
a support substrate of a first conductive-type that is provided beneath the insulating layer; and  
~~a well pattern of one of a first conductive type and a second conductive type that is provided in a predetermined region of the support substrate; and~~  
an interlayer dielectric layer including a conductive layer pattern formed on the support substrate and under the insulating layer.
2. (Original) A semiconductor substrate according to claim 1, wherein a predetermined electric potential is applied to the well pattern via a connection member that passes through the insulating layer.
3. (Original) A semiconductor substrate according to claim 1, wherein the predetermined region where the well pattern is provided includes at least another region where a pad is disposed .

4-10. (Cancelled)

11. (Currently Amended) A semiconductor device comprising:

a support substrate of a predetermined conductive type that is provided with a well pattern formed in a predetermined region;

an insulating layer on the support substrate;

a single-crystal silicon layer on the insulating layer;

an element isolation region selectively formed in the single-crystal silicon layer;

an integrated circuit element arranged in the single-crystal silicon layer;

and

an electrical connection member that passes from the main surface of the integrated circuit element and to the well pattern through the insulating layer; and

an interlayer dielectric layer including a conductive layer pattern formed on the support substrate and under the insulating layer.

12. (Original) The semiconductor device of claim 11, wherein the well pattern controls the electric potential relating to the integrated circuit element.

13. (Original) The semiconductor device of claim 11, wherein the well pattern is used as at least one of a wiring layer and a component in a passive element.

14. (Currently Amended) A semiconductor device comprising:

- a support substrate including a ~~conductive layer~~ well pattern formed in a predetermined region;
- a conductive layer pattern on the support substrate;
- an insulating layer on the support substrate and the conductive layer pattern;
- a single-crystal silicon layer on the insulating layer;
- an element isolation region selectively formed in the single-crystal silicon layer;
- an integrated circuit element arranged upon the single-crystal silicon layer;
- and
- an electrical connection member that passes from the main surface of the integrated circuit element and to the conductive layer pattern through the insulating layer.

15. (Original) The semiconductor device of claim 14, wherein the conductive layer pattern controls the electric potential relating to the integrated circuit element.

16. (Original) The semiconductor device of claim 14, wherein the conductive layer pattern is used as at least one of a wiring layer and a component in a passive element.

17. (Cancelled)